Alunos: Guilherme Amorim, Matheus Silva, Thiago Santos

Tabela 1. Exemplo de um mapa de memória:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Faixa de endereços (hex) | Tamanho da mem. (bytes) | Utilidade da mem | Nome do componente vhd de memória | Tecnologia da mem |
| 0x0000 0B00 – 0x0000 0700 | 1024 B | Memória de dados dinâmica (*stack e heap*) | Mem\_data | RAM |
| 0x0000 06FF – 0x0000 0300 | 1024 B | Memória de dados estática | Mem\_data | RAM |
| 0x0000 02FF – 0x0000 0100 | 512 B | Memória de programa | Mem\_program | FLASH |
| 0x0000 00FF – 0x0000 0000 | 256 B | Periféricos mapeados | Mem\_mapped | RAM |

Tabela2. Exemplo de um detalhamento da região de periféricos do mapa de memória:

|  |  |  |  |
| --- | --- | --- | --- |
| Endereços (hex) | Nome do registrador | Periférico | Mapa em *bits* do registrador |
| 0x0000 00C0 |  |  |  |
| 0x0000 0080 |  |  |  |
| 0x0000 0040 |  |  |  |
| 0x0000 0000 |  |  |  |

**Observação**: o exemplo acima considera que as palavras (e também os registradores) são todos de 32 bits de tamanho (4 bytes) e que o endereçamento dessa CPU é por byte, ou seja, cada byte tem o seu próprio endereço. Portanto, na região de memória reservada para o mapeamento dos registradores dos periféricos, cabe até 64 registradores de 32 bits. Preencha os detalhes da tabela 2, somente quando for implementar os periféricos do seu MCU.

# Etapa 1: Definição de requisitos do projeto

• Quais instruções sua CPU poderá processar, ou seja, o início da definição da ISA:

1. **Arithmetic Instructions:** add, subtract, add immediate;
2. **Logical Instructions:** shift left logical e shift right logical;
3. **Data transfer Instructions:** load word, store word, load byte, store byte;
4. **Conditional branch Instruction:** branch on equal, branch on not equal, set on less than, set less than immediate;
5. **Jump: Instructions:** jump, jump register, jump and link;
6. **Interruption Instruction:** syscall;
7. Nop (no operation).

• Tamanho(s) da instrução:

32 bits.

• Tamanho do(s) dado(s) que a sua CPU será capaz de processar:

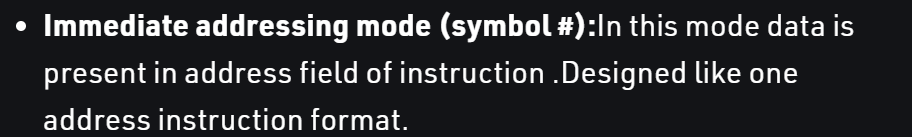
32 bits.

• Capacidade de memória que a sua CPU será capaz de endereçar (tem a ver com o PC):

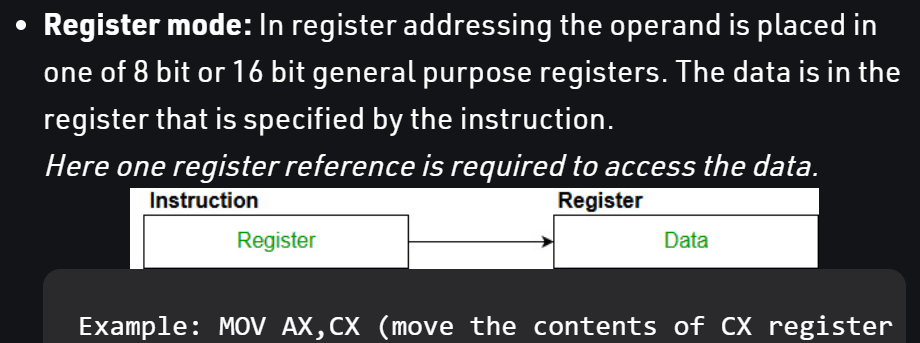
Considerando um *program counter* de 32 bits, no qual somente os 12 bits menos significativos são utilizados no endereçamento:

• Formas de endereçamento que a sua CPU será capaz de tratar:

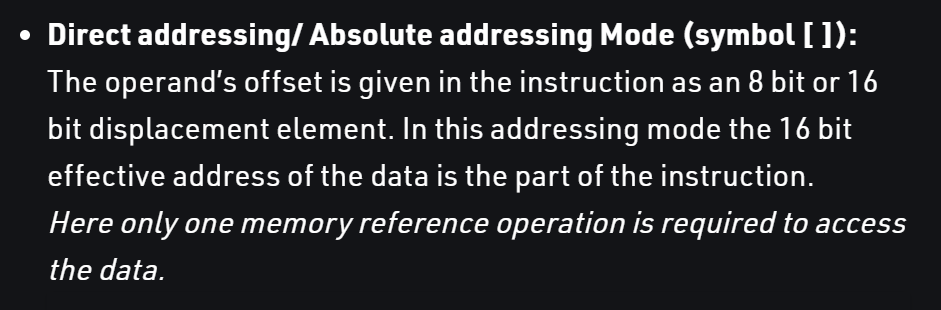
* Endereçamento por imediato (Immediate addressing mode);

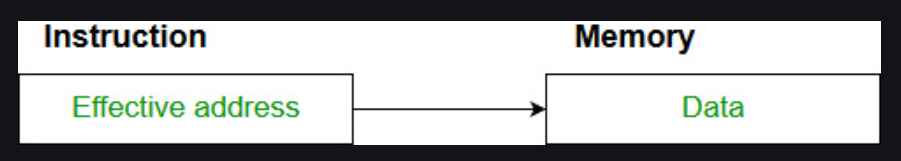


* Endereçamento por registrador (Register mode);

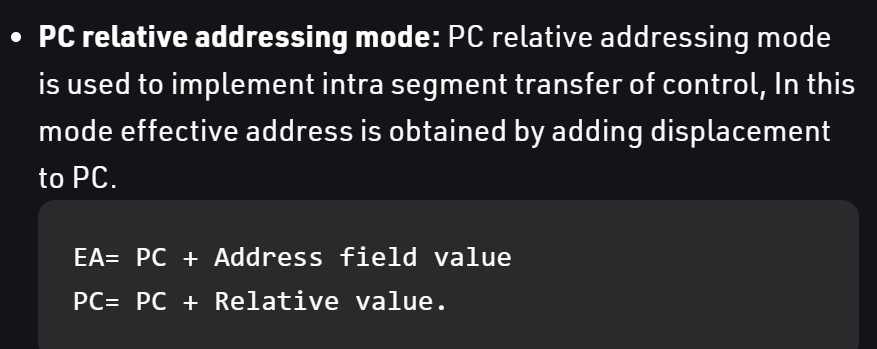


* Endereçamento direto (Direct addressing/ Absolute addressing Mode):

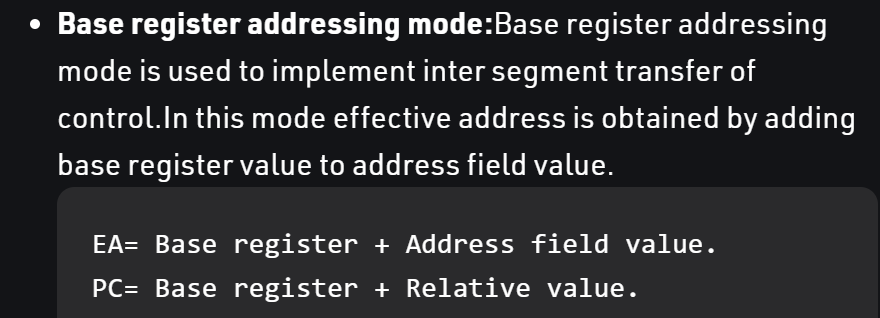




* Endereçamento relativo ao PC (PC relative addressing mode);



* Endereçamento a partir de um registrador base (Base register addressing mode);

]

• Formas de E/S que a sua CPU será capaz de tratar:

Polling e Interrupção.

• Priorizará ou não o uso de banco de registradores no processamento dos dados?

Sim.

• Modelo RISC ou Modelo CISC:

RISC.

• Modelo Von Neumann ou Modelo Harvard:

Modelo Von Neumann.

• Modelo de CPU: ciclo único, multiciclo ou pipeline simples?

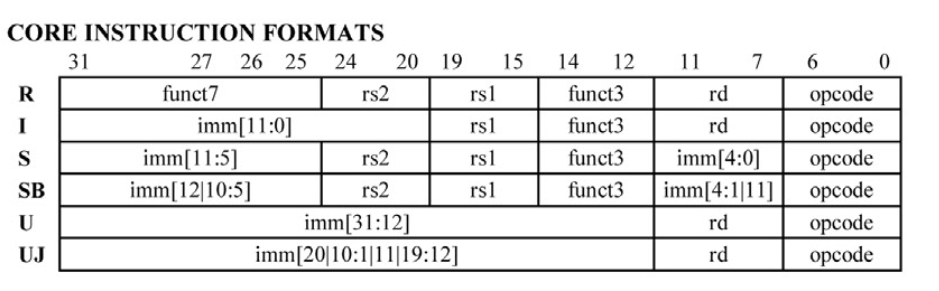
Ciclo único, mas a ideia é posteriormente fazer o pipeline.

• Endianess – ordenamento de bytes dentro da palavra (little endian ou big endian):

Little endian.

# Etapa 2: Detalhamento (ou refinamento) dos requisitos do projeto.

Detalhe cada instrução da ISA do seu processador (equivale ao detalhamento do datasheet do seu processador)



|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| |  |  | | --- | --- | | Mnemônico | ADD | | Mapa de campos da sua instrução | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Rs2 | | | | | Rs1 | | | | | 0 | 0 | 0 | rd | | | | | 0 | 1 | 1 | 0 | 0 | 1 | 1 | | | *Opcode* | 0110011 | | Tamanho da instrução | 32 bits | | Quantidade de operandos | 2 | | Exemplo de uso da instrução | ADD X3 X1 X2 | | Discriminação de cada operando (tamanho e tipo) | R[rd] = R[rs1] + R[rs2]  Rd = Registrador de Destino (5)  Rs1 = Registrador de origem 1 (5)  Rs2 = Registrador de origem 2 (5) | | Tipo de operações que a instrução demanda | Adição de operandos | | Tipo de endereçamento da instrução | Registrador | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| |  |  | | --- | --- | | Mnemônico | SUB | | Mapa de campos da sua instrução | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Rs2 | | | | | Rs1 | | | | | 0 | 0 | 0 | rd | | | | | 0 | 1 | 1 | 0 | 0 | 1 | 1 | | | *Opcode* | 0110011 | | Tamanho da instrução | 32 bits | | Quantidade de operandos | 2 | | Exemplo de uso da instrução | SUB X3 X1 X2 | | Discriminação de cada operando (tamanho e tipo) | R[rd] = R[rs1] - R[rs2]  Rd = Registrador de Destino (5)  Rs1 = Registrador de origem 1 (5)  Rs2 = Registrador de origem 2 (5) | | Tipo de operações que a instrução demanda | Subtração de operandos | | Tipo de endereçamento da instrução | Registrador | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| |  |  | | --- | --- | | Mnemônico | ADDI | | Mapa de campos da sua instrução | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 | | Imm | | | | | | | | | | | | Rs1 | | | | | 0 | 0 | 0 | rd | | | | | 0 | 0 | 1 | 0 | 0 | 1 | 1 | | | *Opcode* | 0010011 | | Tamanho da instrução | 32 bits | | Quantidade de operandos | 2 | | Exemplo de uso da instrução | ADDI X3 X1 5 | | Discriminação de cada operando (tamanho e tipo) | R[rd] = R[rs1] + Imm  Rd = Registrador de Destino (5)  Rs1 = Registrador de origem 1 (5)  Imm = Imediato (12) | | Tipo de operações que a instrução demanda | Adição entre um operando e um valor imediato | | Tipo de endereçamento da instrução | Registrador | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| |  |  | | --- | --- | | Mnemônico | SLL | | Mapa de campos da sua instrução | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Rs2 | | | | | Rs1 | | | | | 0 | 0 | 1 | rd | | | | | 0 | 1 | 1 | 0 | 0 | 1 | 1 | | | *Opcode* | 0110011 | | Tamanho da instrução | 32 bits | | Quantidade de operandos | 2 | | Exemplo de uso da instrução | SLL X3 X1 X2 | | Discriminação de cada operando (tamanho e tipo) | R[rd] = R[rs1] << R[rs2]  Rd = Registrador de Destino (5)  Rs1 = Registrador de origem 1 (5)  Rs2 = Registrador de origem 2 (5) | | Tipo de operações que a instrução demanda | Deslocamento de bits para a esquerda | | Tipo de endereçamento da instrução | Registrador | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| |  |  | | --- | --- | | Mnemônico | SRL | | Mapa de campos da sua instrução | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Rs2 | | | | | Rs1 | | | | | 1 | 0 | 1 | rd | | | | | 0 | 1 | 1 | 0 | 0 | 1 | 1 | | | *Opcode* | 0110011 | | Tamanho da instrução | 32 bits | | Quantidade de operandos | 2 | | Exemplo de uso da instrução | SRL X3 X1 X2 | | Discriminação de cada operando (tamanho e tipo) | R[rd] = R[rs1] >> R[rs2]  Rd = Registrador de Destino (5)  Rs1 = Registrador de origem 1 (5)  Rs2 = Registrador de origem 2 (5) | | Tipo de operações que a instrução demanda | Deslocamento de bits para a direito | | Tipo de endereçamento da instrução | Registrador | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| |  |  | | --- | --- | | Mnemônico | LW | | Mapa de campos da sua instrução | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 | | Imm | | | | | | | | | | | | X | | | | | 0 | 1 | 0 | rd | | | | | 0 | 0 | 0 | 0 | 0 | 1 | 1 | | | *Opcode* | 0000011 | | Tamanho da instrução | 32 bits | | Quantidade de operandos | 2 | | Exemplo de uso da instrução | LW X3 5 | | Discriminação de cada operando (tamanho e tipo) | R[rd] = M[Imm]  Rd = Registrador de Destino (5)  X = Don’t care  Imm = Imediato (12) | | Tipo de operações que a instrução demanda | Carrega uma word de dados da memória para o registrador. | | Tipo de endereçamento da instrução | Direto | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| |  |  | | --- | --- | | Mnemônico | SW | | Mapa de campos da sua instrução | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 | | Imm | | | | | | | | | | | | X | | | | | 0 | 1 | 0 | rd | | | | | 0 | 1 | 0 | 0 | 0 | 1 | 1 | | | *Opcode* | 0100011 | | Tamanho da instrução | 32 bits | | Quantidade de operandos | 2 | | Exemplo de uso da instrução | SW X3 5 | | Discriminação de cada operando (tamanho e tipo) | M[Imm] = R[rd]  Rd = Registrador de Destino (5)  X = Don’t care  Imm = Imediato (12) | | Tipo de operações que a instrução demanda | Carrega uma word de dados do registrador para a memória. | | Tipo de endereçamento da instrução | Direto | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| |  |  | | --- | --- | | Mnemônico | LB | | Mapa de campos da sua instrução | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 | | Imm | | | | | | | | | | | | X | | | | | 0 | 0 | 0 | rd | | | | | 0 | 0 | 0 | 0 | 0 | 1 | 1 | | | *Opcode* | 0000011 | | Tamanho da instrução | 32 bits | | Quantidade de operandos | 2 | | Exemplo de uso da instrução | LB X3 5 | | Discriminação de cada operando (tamanho e tipo) | R[rd] = M[Imm]  Rd = Registrador de Destino (5)  X = Don’t care  Imm = Imediato (12) | | Tipo de operações que a instrução demanda | Carrega um byte de dados da memória para o registrador. | | Tipo de endereçamento da instrução | Direto | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| |  |  | | --- | --- | | Mnemônico | SB | | Mapa de campos da sua instrução | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 | | Imm | | | | | | | | | | | | X | | | | | 0 | 0 | 0 | rd | | | | | 0 | 1 | 0 | 0 | 0 | 1 | 1 | | | *Opcode* | 0100011 | | Tamanho da instrução | 32 bits | | Quantidade de operandos | 2 | | Exemplo de uso da instrução | SB X3 5 | | Discriminação de cada operando (tamanho e tipo) | M[Imm] = R[rd]  Rd = Registrador de Destino (5)  X = Don’t care  Imm = Imediato (12) | | Tipo de operações que a instrução demanda | Carrega um byte de dados do registrador para a memória. | | Tipo de endereçamento da instrução | Direto | |

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| |  |  | | --- | --- | | Mnemônico | BEQ | | Mapa de campos da sua instrução | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 | | Imm | | | | | | | | | | | | Rs1 | | | | | 0 | 1 | 0 | Rs2 | | | | | 0 | 1 | 0 | 0 | 0 | 1 | 1 | | | *Opcode* | 0100011 | | Tamanho da instrução | 32 bits | | Quantidade de operandos | 2 | | Exemplo de uso da instrução | BEQ X1 X2 32 | | Discriminação de cada operando (tamanho e tipo) | PC = (R[s1] == R[s2]) ? PC+IMM : PC  Rs1 = Registrador de origem 1 (5)  Rs2 = Registrador de origem 2 (5)  PC = Program counter  Imm = Imediato (12) | | Tipo de operações que a instrução demanda | Efetua um branch condicional (igualdade). | | Tipo de endereçamento da instrução | Referente a PC | |

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| |  |  | | --- | --- | | Mnemônico | BNE | | Mapa de campos da sua instrução | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 | | Imm | | | | | | | | | | | | Rs1 | | | | | 0 | 0 | 1 | Rs2 | | | | | 0 | 1 | 0 | 0 | 0 | 1 | 1 | | | *Opcode* | 0100011 | | Tamanho da instrução | 32 bits | | Quantidade de operandos | 2 | | Exemplo de uso da instrução | BNE X1 X2 32 | | Discriminação de cada operando (tamanho e tipo) | PC = (R[s1] != R[s2]) ? PC+IMM : PC  Rs1 = Registrador de origem 1 (5)  Rs2 = Registrador de origem 2 (5)  PC = Program counter  Imm = Imediato (12) | | Tipo de operações que a instrução demanda | Efetua um branch condicional (desigualdade). | | Tipo de endereçamento da instrução | Referente a PC | |

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| |  |  | | --- | --- | | Mnemônico | SLT | | Mapa de campos da sua instrução | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Rs2 | | | | | Rs1 | | | | | 0 | 1 | 0 | rd | | | | | 0 | 1 | 1 | 0 | 0 | 1 | 1 | | | *Opcode* | 0110011 | | Tamanho da instrução | 32 bits | | Quantidade de operandos | 2 | | Exemplo de uso da instrução | SLT X3 X1 X2 | | Discriminação de cada operando (tamanho e tipo) | R[rd] = (R[rs1] < R[rs2]) ? 1 : 0  Rd = Registrador de Destino (5)  Rs1 = Registrador de origem 1 (5)  Rs2 = Registrador de origem 2 (5) | | Tipo de operações que a instrução demanda | Coloca o nível logico no registrador de saída de acordo com os sinais de entrada.  Caso o valor armazenado no registrador um for menor que presente no registrador dois, teremos nível alto na saída  e no caso contrário nível baixo | | Tipo de endereçamento da instrução | Registrador | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| |  |  | | --- | --- | | Mnemônico | SLTI | | Mapa de campos da sua instrução | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 | | Imm | | | | | | | | | | | | Rs1 | | | | | 0 | 1 | 0 | rd | | | | | 0 | 0 | 1 | 0 | 0 | 1 | 1 | | | *Opcode* | 0010011 | | Tamanho da instrução | 32 bits | | Quantidade de operandos | 2 | | Exemplo de uso da instrução | SLTI X3 X2 5 | | Discriminação de cada operando (tamanho e tipo) | R[rd] = (R(rs1) < Imm) ? 1 : 0  Rd = Registrador de Destino (5)  Rs1 = Registrador de origem 1 (5)  Imm = Imediato (12) | | Tipo de operações que a instrução demanda | Coloca o nível logico no registrador de saída de acordo com os sinais de entrada.  Caso o valor armazenado no registrador um for menor que presente imediato, teremos nível alto na saída  e no caso contrário nível baixo | | Tipo de endereçamento da instrução | Registrador | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| |  |  | | --- | --- | | Mnemônico | J | | Mapa de campos da sua instrução | |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 | | Imm | | | | | | | | | | | | | | | | | | | | | | | | | 0 | 0 | 0 | 0 | 0 | 1 | 0 | | | *Opcode* | 0000010 | | Tamanho da instrução | 32 bits | | Quantidade de operandos | 1 | | Exemplo de uso da instrução | J 50 | | Discriminação de cada operando (tamanho e tipo) | PC[31 : 0] = PC[31:28] + Imm + 00  PC = Program counter (31)  PC[31:28] = quatro bits mais significativos do PC original  Imm = Imediato (26)  00 = dois últimos bits do PC final | | Tipo de operações que a instrução demanda | Atualiza o program counter, garantindo um desvio de fluxo para a instrução indicada pelo imediato | | Tipo de endereçamento da instrução | Registrador | |

• Mnemônico

• Tamanho da instrução

• Mapa de campos da sua instrução

• Opcode: um código binário único associado a cada instrução.

• Quantidade e tipos de operandos

• Tamanho de cada operando

• Tipo de operações que a instrução demanda

• Tipo de endereçamento da instrução

Referências:

* https://www.geeksforgeeks.org/addressing-modes/